New Application: Yuji FUJIKI
Filed: August 20, 2003
9 sheets of drawings FIGS.1-9
RABIN & BERDO, P.C.
Atty Docket: OKI 367
Customer NO.: 23995

F-01ED0546

FIG. 1

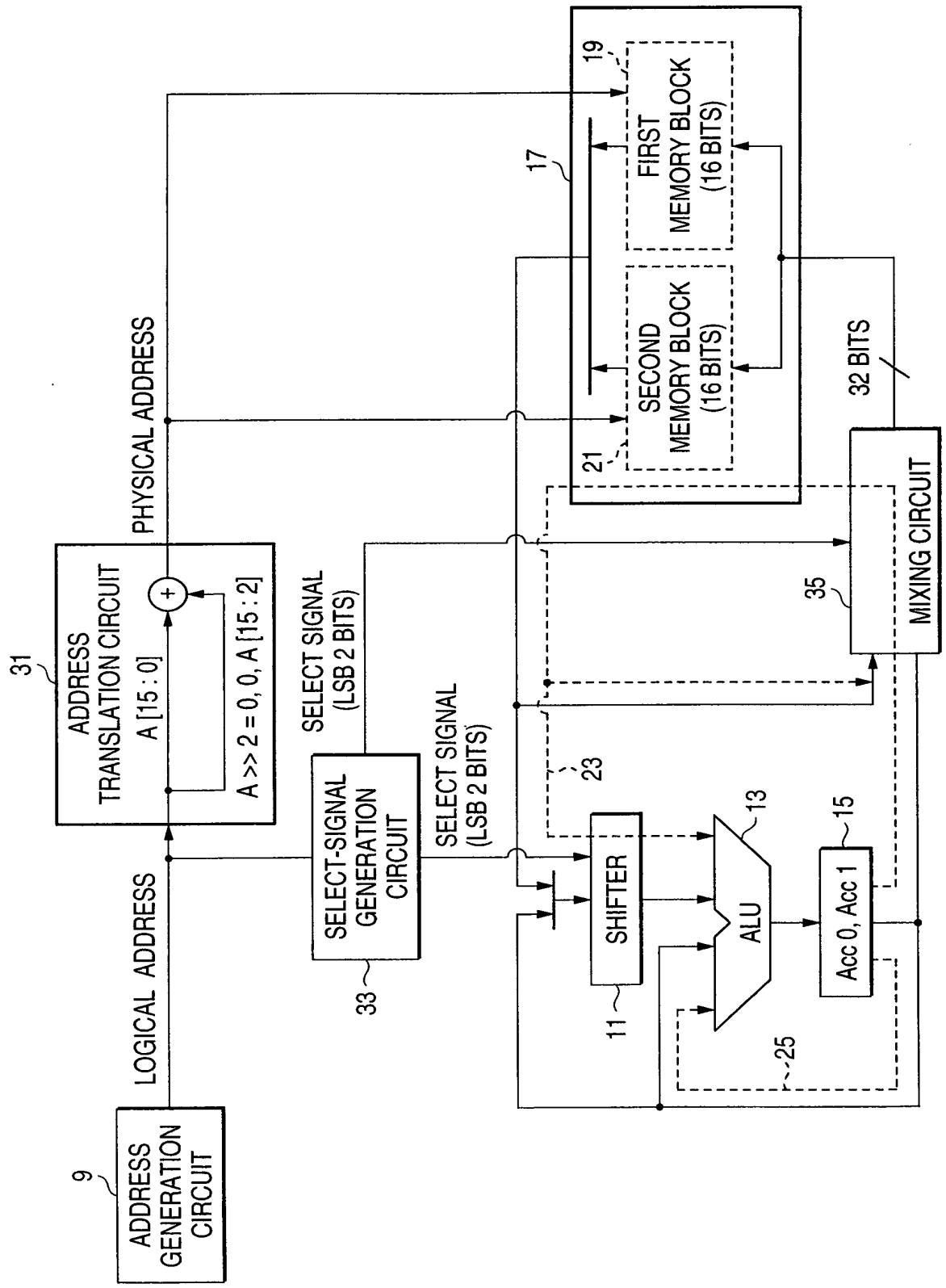

FIG. 2

FIRST MEMORY BLOCK

ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R0 [5 : 0]						I0 [9 : 0]									
2	R1 [5 : 0]						I1 [9 : 0]									
4	R2 [5 : 0]						I2 [9 : 0]									
6	R3 [5 : 0]						I3 [9 : 0]									
8	R4 [5 : 0]						I4 [9 : 0]									
10	R5 [5 : 0]						I5 [9 : 0]									
12	R6 [5 : 0]						I6 [9 : 0]									
14	R7 [5 : 0]						I7 [9 : 0]									
16	R8 [5 : 0]						I8 [9 : 0]									
18	R9 [5 : 0]						I9 [9 : 0]									

SECOND MEMORY BLOCK

ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	RESERVED DATA												R0 [9 : 6]			
3	RESERVED DATA												R1 [9 : 6]			
5	RESERVED DATA												R2 [9 : 6]			
7	RESERVED DATA												R3 [9 : 6]			
9	RESERVED DATA												R4 [9 : 6]			
11	RESERVED DATA												R5 [9 : 6]			
13	RESERVED DATA												R6 [9 : 6]			
15	RESERVED DATA												R7 [9 : 6]			
17	RESERVED DATA												R8 [9 : 6]			
19	RESERVED DATA												R9 [9 : 6]			
	RESERVED DATA															
	RESERVED DATA															

FIG. 3

FIRST MEMORY BLOCK

ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	R0 [5 : 0]						I0 [9 : 0] ▲									
2	I2 [7 : 0] ▲								R1 [9 : 2]							
4	R3 [9 : 0]										I3 [9 : 4]					
6	R5[1:0]	I5 [9 : 0] ▲										R4 [9 : 6]				
8	I7 [3 : 0] ▲			R6 [9 : 0]											I6 [9:8]	
10	R8 [5 : 0]						I8 [9 : 0] ▲									
12	I10 [7 : 0] ▲								R9 [9 : 2]							

▲ : HEAD ADDRESS OF Ix

SECOND MEMORY BLOCK

ADDRESS	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	R1[1:0]				I1 [9 : 0] ▲								R0 [9 : 6]			
3	I3 [3 : 0] ▲				R2 [9 : 0]										I2 [9:8]	
5	R4 [5 : 0]						I4 [9 : 0] ▲									
7	I6 [7 : 0] ▲								R5 [9 : 2]							
9	R7 [9 : 0]										I7 [9 : 4]					
11	R9[1:0]	I9 [9 : 0] ▲										R8 [9 : 6]				
13	I11 [3 : 0] ▲				R10 [9 : 0]										I10[9:8]	

▲ : HEAD ADDRESS OF Ix

FIG. 4

LOGICAL ADDRESS (a)	CALCULATION FORMULA: LOGICAL ADDRESS + (LOGICAL ADDRESS) >> 2	PHYSICAL ADDRESS (A)
0	0/2 + [(0/2)/4] = 0 + 0 = 0	0
2	2/2 + [(2/2)/4] = 1 + 0 = 1	1
4	4/2 + [(4/2)/4] = 2 + 0 = 2	2
6	6/2 + [(6/2)/4] = 3 + 0 = 3	3
8	8/2 + [(8/2)/4] = 4 + 1 = 5	5
10	10/2 + [(10/2)/4] = 5 + 1 = 6	6
12	12/2 + [(12/2)/4] = 6 + 1 = 7	7
14	14/2 + [(14/2)/4] = 7 + 1 = 8	8
16	16/2 + [(16/2)/4] = 8 + 2 = 10	10
18	18/2 + [(18/2)/4] = 9 + 2 = 11	11

FIG. 5

LOGICAL ADDRESS (a)	LSB 2 BITS	CALCULATION FORMULA: LSB 2 BITS x 4	SHIFT MAGNITUDE (B)
0	0	0 x 4 = 0	0
2	1	1 x 4 = 4	4
4	2	2 x 4 = 8	8
6	3	3 x 4 = 12	12
8	0	0 x 4 = 0	0
10	1	1 x 4 = 4	4
12	2	2 x 4 = 8	8
14	3	3 x 4 = 12	12
16	0	0 x 4 = 0	0
18	1	1 x 4 = 4	4

FIG. 6

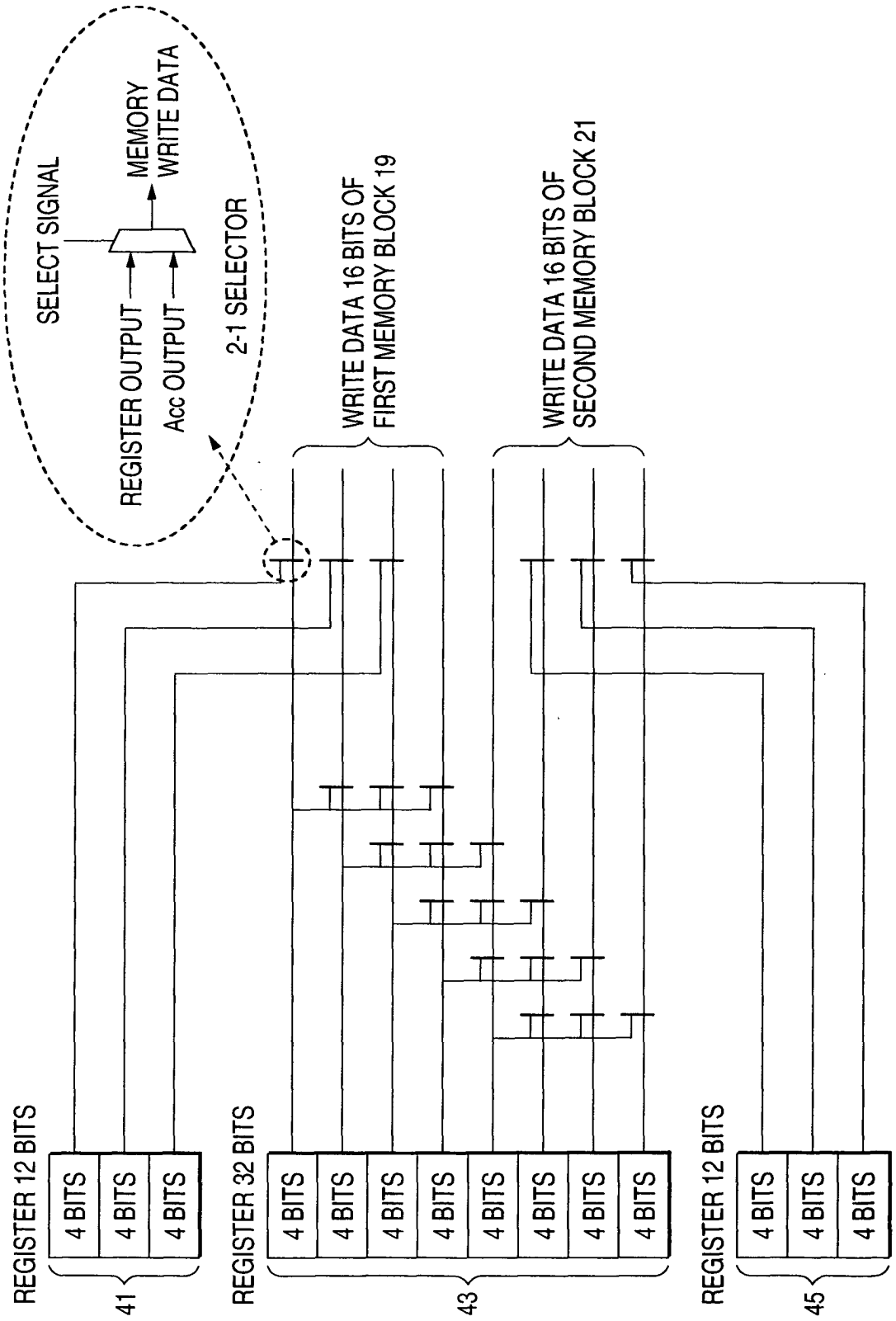
SELECT SIGNAL
MEMORY WRITE DATA
REGISTER OUTPUT
Acc OUTPUT
2-1 SELECTOR
WRITE DATA 16 BITS OF FIRST MEMORY BLOCK 19
WRITE DATA 16 BITS OF SECOND MEMORY BLOCK 21
REGISTER 12 BITS
4 BITS
4 BITS
4 BITS
41
REGISTER 32 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
43
REGISTER 12 BITS
4 BITS
4 BITS
4 BITS
45

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FIG. 7

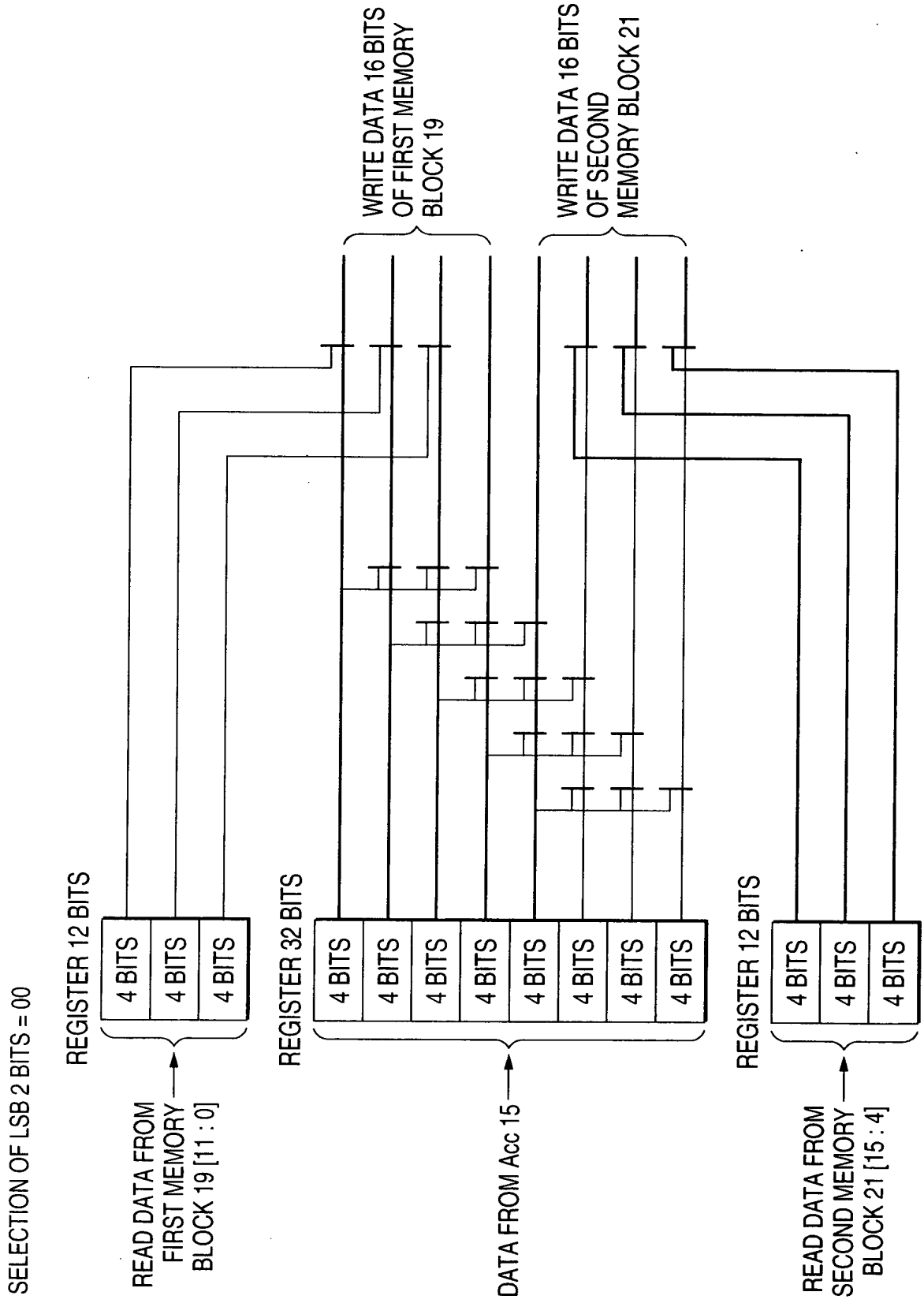

FIG. 8

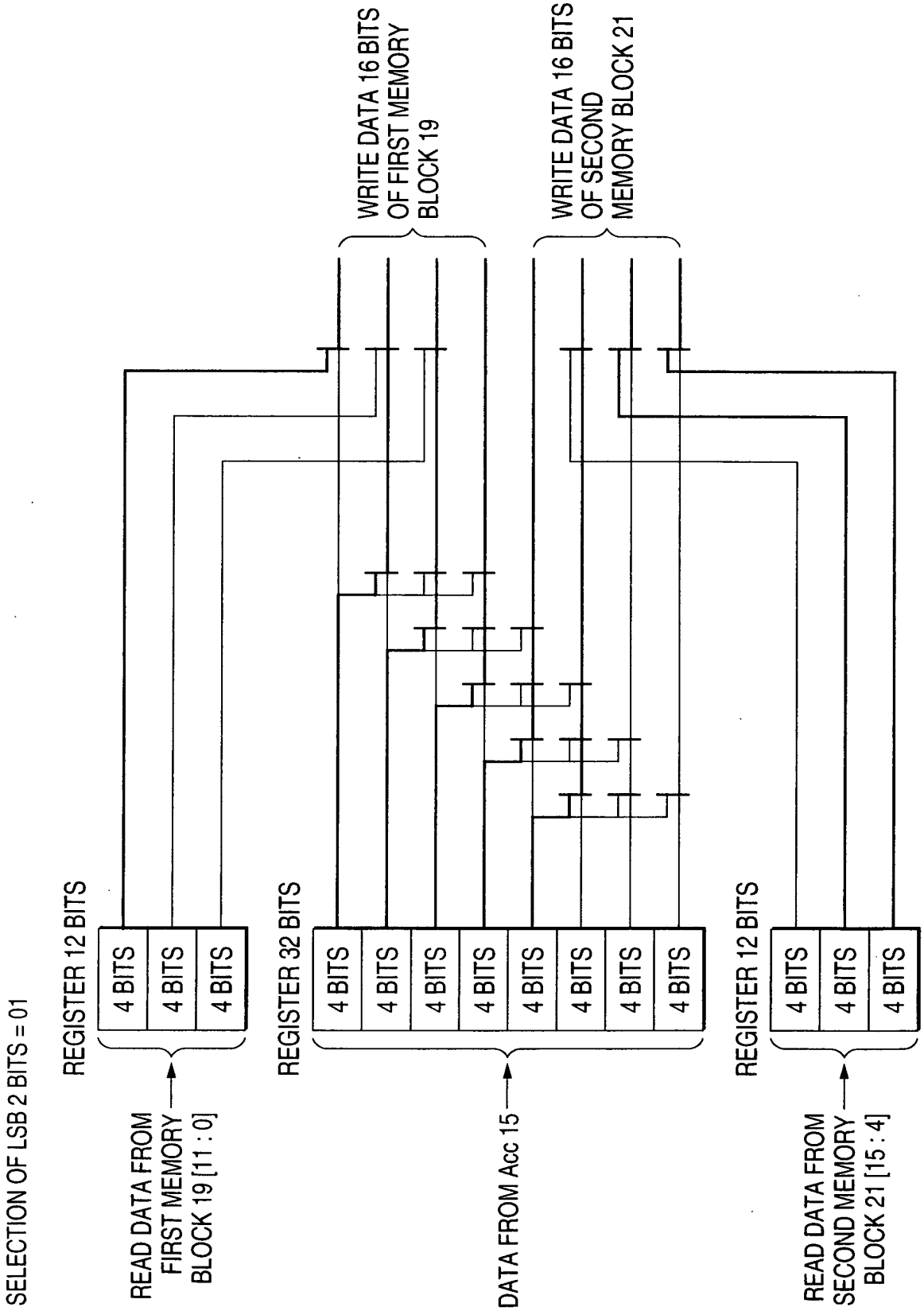
SELECTION OF LSB 2 BITS = 01
REGISTER 12 BITS
4 BITS
4 BITS
4 BITS
READ DATA FROM FIRST MEMORY BLOCK 19 [11 : 0]
REGISTER 32 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
4 BITS
DATA FROM Acc 15
REGISTER 12 BITS
4 BITS
4 BITS
4 BITS
READ DATA FROM SECOND MEMORY BLOCK 21 [15 : 4]
WRITE DATA 16 BITS OF FIRST MEMORY BLOCK 19
WRITE DATA 16 BITS OF SECOND MEMORY BLOCK 21

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FIG. 9